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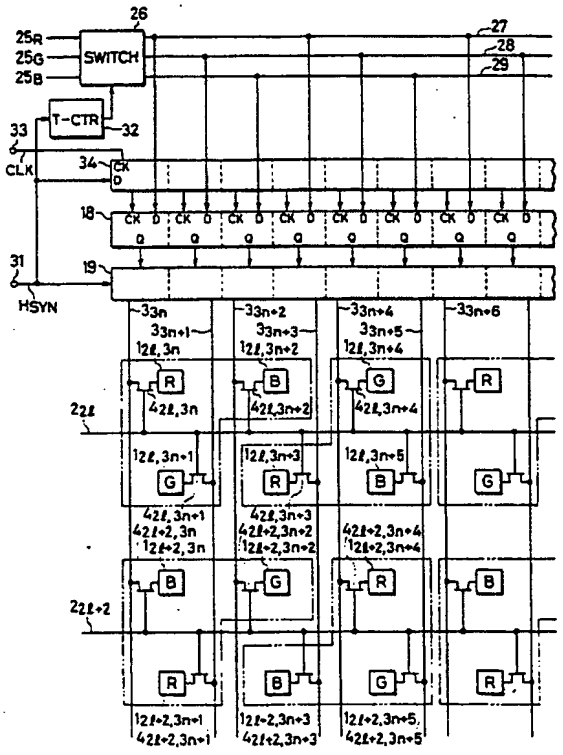
## (54) Planar display device.

(57) A planar display device is disclosed, which comprises a plurality of display elements ($1_{2\ell}$,3n) in rows and columns, row drive lines ($2_{2\ell}$) each commonly connected to two adjacent rows of display elements and column drive lines ($3_{3n}$, $3_{3n+1}$) provided in pairs each for each column of display elements every other ones of the display elements in the column being connected to one of the pair column drive lines, the other display elements in the column being connected to the other column drive lines in the pair. Each of the display elements is selectively activated by the row and column drive lines connected thereto.

FIG. 9

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# PLANAR DISPLAY DEVICE

## BACKGROUND OF THE INVENTION

This invention relates to a planar display device for displaying a monochromatic or color image as liquid crystal display, plasma display, light-emitting diode display, etc. with a plurality of display elements arranged in rows and columns.

As the prior art, a color liquid crystal display device will be described to point out problems in this type of planar display device.

Referring to Fig. 1, there is shown a liquid crystal display device, which comprises a pair of transparent sunbstrates 11 and 12 and liquid crystal 13 sealed therebetween. A plurality of tranparent square display electrodes $1_{\ell,n}$($\ell$ = 1, 2, 3, ••• , n = 1, 2, 3, ••• ) are provided on the inner surface of one of the transparent substrates, i.e., substrate 11. A transparent common electrode 14 is provided on the entire inner surface of the other substrate 12.

The display electrodes $1_{\ell,n}$ are arranged in rows and columns. As shown in Fig. 2, a row drive line $2_\ell$ is provided along corresponding one of rows of display electrodes $1_{\ell,n}$, and a column drive line $3_n$ is provided along corresponding one of columns of display electrodes $1_{\ell,n}$. A thin-film transistor $4_{\ell,n}$is provided for each display electrode $1_{\ell,n}$. Each thin-film transistor $4_{\ell,n}$has a drain connected to the corresponding display electrode $1_{\ell,n}$, a gate connected to the corresponding row drive line $2_\ell$and a source connected to the corresponding column drive line $3_n$. Thus, when one row drive line $2_\ell$ and one column drive line $3_n$ are selectively drive, only the thin-film transistor $1_{\ell,n}$ connected to these row and column lines is turned on, i.e., rendered conductive. The corresponding display electrode $1_{\ell,n}$ is thus connected to the column drive line $3_n$, and a voltage is applied between the display electrode $1_{\ell,n}$ and the common electrode 14 (Fig. 1). The pertaining portion of the liquid crystal 13 thus is controlled so that it is rendered to have different light transmission characteristics from those of the rest of the liquid crystal. In this manner, voltage is selectively applied to the plurality of display electrodes $1_{\ell,n}$according to an image to be displayed, whereby a monochromatic pixel display is obtained. Each of the display electrodes $1_{\ell,n}$ corresponding one of the thin-film transistors $4_{\ell,n}$, corresponding portion of liquid crystal 13 and common electrode 14 constitute, in all, one of display elements $5_{\ell,n}$.

For the color display, a red filter R, a green filter G and a blue filter B are provided on either respective display electrodes $1_{\ell,n}$ or on the corresponding portions of the common electrode 14. These color filters are arranged substantially uniformly, for instance as shown in Fig. 3. Various colors can be displayed as mixtures of the red, green and blue colors depending on the state of display by the plurality of display elements corresponding to the respective display electrodes. Hereinunder, the display elements for displaying the red color will be referred to as R, the display elements for displaying the green color as G, and the display elements for displaying the blue color as B.

For displaying a white picture point (i.e., a white dot) on the planar color display device, three display elements, i.e., red, green and blue display elements, adjacent to one another, have to be driven simultaneously for white color emission. White horizontal and vertical lines can be displayed simply by activating corresponding row and column of display elements R, G and B. A 45-degree white oblique line from the right top to the left bottom of the display device can also be displayed by selectively activating display elements R, G and B along the oblique line, as shown in Fig. 4. However, when display elements are selected along a 45-degree oblique line from the left top to the right bottom on the display device, only one of the three colors, e.g. red display elements R are displayed and a white line can not be display, as shown in Fig. 5. This problem arises if it is intended to have one picture element (i.e., pixel) constituted by one display element, i.e., if each display element is intended to be used as a resolvable picture element so that a thin oblique or curved display line can be achieved.

From this standpoint, it is desired to adopt a three-color display element set for a picture dot, in which a set of three adjacent color display elements, i.e. red, green and blue color display elements R, G and B, are simultaneously driven for display of a white picture point, and also any other desired color is displayed as a picture point (i.e., dot) of a resultant color of suitable combination of light intensities through the three color display elements. To this end, one may occur to consider of forming sets of color display elements using each two adjacent rows of color display elements as shown in Fig. 6. More specifically, it can be arranged to have adjacent red, green and blue display elements R, G and B in two adjacent element rows as a set, as shown in Fig. 6, thus defining color display element sets each shown enclosed by a phantom line, these sets constituting respective picture points $P_{i,j}$(i = 1, 2, 3, ••• , j = 1, 2, 3, •••)

For the display on the planar display device, one row drive line $2_\ell$ is selectively driven via a row drive circuit 17 according to the contents of a row register 16, while one column drive line $3_n$ is selectively driven via a column drive circuit 19 according to the contents of a column register 18, as shown in Fig. 2, thus causing the display of a corresponding display electrode. In the column register 18, image signal data for one display line is stored in correspondence to individual display elements $5_{\ell,n}$ of the display line. After the display of this line, the next row drive line is selectively driven, and image signal data for the next line of display element row to be displayed is stored in the column register 18. Likewise, successive row drive lines are selectively driven while storing image signal data for a line in the column register 18 after selection of each row drive line.

For the display through representation by sets of three-color display elements as respective picture points as shown in Fig. 6 using the system of Fig. 2, one display row $6_i$ is displayed as follows. As the image signal, three color signals $R_k$, $G_k$ and $B_k$ ($k = 1, 2, 3, \bullet\bullet\bullet$) for each picture point (i.e., dot) are supplied as parallel signals, as shown in Fig. 7. The individual picture point signals in the signals for one display row are divided into two signals, i.e., one being a stream of $R_1$, $B_1$, $C_2$, $R_3$, $B_3$, $G_4$, $\bullet\bullet\bullet$ loaded in the column register 18 as shown in Fig. 8A and the other being a stream of $G_1$, $R_2$, $B_2$, $G_3$, $R_4$, $B_4$, $\bullet\bullet\bullet$ as shown in Fig. 8B. First, the signal shown in Fig. 8A stored in the column register 18 in Fig. 2 is provided to activate the display elements connected to the corresponding row drive line $2_\ell$ and individual column drive lines $3_n$, $3_{n+1}$, $2_{n+2}$, $\bullet\bullet\bullet$ . Then, the signal shown in Fig. 8B stored in the column register 18 is provided to activate the display elements connected to the row drive line $2_\ell + 1$. In the above way, the display signal for one display row (i.e., one horizontal scanning line cycle) is divided into two signals for driving display elements independently. Therefore, the operation is complicated. Besides, since the image signal is usually supplied for each display row, i.e., each horizontal scanning line, the aforementioned display system, therefore, is inferior in view of the matching with the divided two streams of input image signals.

Furthermore, in the planar display device the display surface is repeatedly scanned by selecting successsive row drive lines. If the repetition cycle period of scanning the display area (i.e., vertical cycle period), i.e., one frame display period, is long, flicker of the display surface screen occurs to deteriorate the quality of display. For this reason, it is difficult to set the vertical cycle period to be longer than about 1/50 second. Since the vertical cycle period is fixed, by increasing the row drive lines the period of driving one row drive line is reduced. Therefore, this leads to a problem in case of a liquid crystal display drive in that display electrodes fail to be charged sufficiently. That is, there is an upper limit on the number of row drive lines, and the resolution can not be improved beyond this limit. Even in case of a display device having high response speed compared to the liquid crystal display device, increasing the row drive lines dictates increase in the rate of switching of the tow drive lines, thus leading to expensive and complicated peripheral circuits.

## SUMMARY OF THE INVENTION

It is an object of the present invention to provide a planar display device which is capable of displaying a picture of graphic pattern with high quality..

According to the invention, row drive lines are each provided for two adjacent rows of display elements. That is, the display elements in the two rows are connected to the common row drive line. Column drive lines are provided in pairs each for each column of display elements. Every other ones of the display elements in the column are connected to one of the pair column drive lines, and the other display elements in the column are connected to the other column drive lines in the pair. Each of the display elements is selectively displayed by the row and column drive lines connected to it.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view showing, in a simplified form, the general construction of a liquid crystal display device;

Fig. 2 is a view showing the relation among display electrodes, drive lines and thin-film transistors of a prior art liquid crystal display device.

Fig. 3 is a view showing an example of arrangement of color filters in the liquid crystal display device;

Fig. 4 is a view showing a 45° display line of an array of display elements extending upper right to lower left;

Fig. 5 is a view showing a 45° display line of an array of display elements extending upper left to lower right;

Fig. 6 is a view showing an example of display as three-color display-element sets as picture dots;

Fig. 7 is a view showing an example of image signal train;

Figs. 8A and 8B show streams of divided image signal stored in the column register 18 for activation of three-color display-element sets as respective picture dots on the prior art display device shown in Fig. 2;

Fig. 9 is a view showing the relation among display electrodes, column drive lines, row drive lines and thin-film transistors in case where a planar display device according to the invention is applied to the liquid crystal display;

Figs 10A, 10B and 10C show an example of a color image signal stored in the column register 18 shown in Fig. 9;

Fig. 11 is a view similar to Fig. 9 but showing a second embodiment of the invention;

Fig. 12 is a view showing a different example of a circuit for supplying an image signal to the display device according to the invention;

Fig. 13 is a view showing an example of interlaced scanning in the second embodiment;

Fig. 14 is a view showing the relation among a liquid crystal AC drive signal, each field and column and row drive lines; and

Fig. 15 is a view showing an example of circuit for producing the AC drive waveform shown in Fig. 14.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, an embodiment of the invention applied to a liquid crystal planar display device will be described. The embodiment employs the structure shown in Fig. 1. However, the embodiment is different from the prior art system in the arrangement and interconnection of the display electrodes and row and column drive lines. Fig. 9 is a view similar to Fig. 2 but shows the embodiment of the invention. Referring to Fig. 9, display electrodes $1_{2\ell,3n}$ are arranged in rows and columns. Unlike the prior art system, row drive lines $2_{2\ell}$ are each provided for two adjacent rows of display electrodes $1_{2\ell,3n}$. In the illustrated example, one row of display electrodes $1_{2\ell,3n}$, $1_{2\ell,3n+2}$, ••• is provided above the row drive line $2_{2\ell}$, and the other row of display electrodes $1_{2\ell,3n+1}$, $1_{2\ell,3n+3}$, ••• is provided below the line. Two column drive lines are provided for each column of display electrodes. For example, column drive lines $3_{3n}$ and $3_{3n+1}$ are provided on the opposite sides of the column of display electrodes $1_{2\ell,3n}$, $1_{2\ell,3n+1}$, ••• .

Thin-film transistors $4_{2\ell,3n}$ are each provided for each of the display electrtodes $1_{2\ell,3n}$. To the row drive line $2_{2\ell}$ are connected the gates of thin-film transistors corresponding to the display electrodes, between which the drive line $2_{2\ell}$ extends. The display electrodes in each column are connected alternately and through the respective thin-film transistors to the column drive lines on the opposite sides of the column. For example, the display electrodes $1_{2\ell,3n}$, $1_{2\ell+2,3n}$ are connected through the respective thin-film transistors $4_{2\ell,3n}$, $4_{2\ell+2,3n}$, ••• to the column line $3_{3n}$, and the display electrodes $1_{2\ell,3n+1}$, $1_{2\ell+2,3n+1}$, ••• are connected through the respective thin-film transistors $4_{2\ell,3n+1}$, $4_{2\ell+2,3n+1}$, ••• to the column drive line $3_{3n+1}$. Again in this structure, each display electrode constitutes together with the corresponding thin-film transistor and corresponding portions of the liquid crystal and common electrode (Fig. 1) a display element 5.

In the case of the color display, red, green and blue color filters R, G and B are provided substantially in a uniform arrangement in correspondence to the individual pixel electrodes.

In this construction, the red, green and blue colour signals $R_k$, $G_k$ and $B_k$ or color image signal supplied through input lines 25R, 25G and 25B are supplied through a color signal switching circuit 26 to color signal buses 27 to 29. A horizontal sync pulse signal $H_{syn}$ of the color image signal is supplied from a horizontal sync input terminal 31 to a tertiary counter 32. The color signal switching circuit 26 is controlled to switch the color signals according to the count of the tertiary counter 32. According to the control the color signal switching circuit 26 connects the input signal lines 25R, 25G and 25B to the color signal buses 27, 28 and 29 , or 28, 29 and 27, or 29, 27 and 28, respectively.

The color signal buses 27 to 29 are repeatedly connected to successive stages of the column register 18, and the outputs of these stages drive the column drive lines $3_{3n}$, $3_{3n+1}$, $3_{3n+2}$, $3_{3n+3}$, $3_{3n+4}$, $3_{3n+5}$, ••• through the column drive circuit 19. A clock signal having three times the dot frequency of the input color image signal is supplied as shift clock from a clock terminal 33 to a shift register 34, and a horizontal sync pulse is supplied from the terminal 31 to the first stage of the shift register 34 at the start of each horizontal scanning cycle period. Data from the individual stages of the column register 18 are fetched successively in response to the outputs of the respective shift stages of the shift register 34.

Thus, when red, green and blue color signals $R_k$, $G_k$ and $B_k$ are stored as the image signal of a certain horizontal cycle period in the manner as shown in Fig. 10A in the column register 18 and the row drive line $2_{2\ell}$ is driven at this time, all the display elements (i.e., display electrodes) in the two rows associated with the row drive line $2_{2\ell}$ shown in Fig. 9 are driven according to the contents of the corresponding stages of the column register 18. Thus, the three-color display-element

sets of respective picture are simultaneously driven for one display row.

In the next horizontal cycle, color signals are stored in the manner as shown in Fig. 10B in the column register 18, and the row drive line $2_2\ell+2$ is driven. Thus, the display elements associated with the row drive line $2_2\ell+2$ shown in Fig. 9 are driven likewise as simultaneous drive for one display row. In the further horizontal cycle, color signals are stored in the manner as shown in Fig. 10C in the column register 18, and the row drive line $2_2\ell+4$ is driven. Thus, the display elements associated with the row drive line $2_2\ell+4$ are driven as simultaneous drive for one display row. The image signal is stored successively and repeatedly in the order of Figs. 10A to 10C for respective horizontal periods in the column register 18. It is possible to arrange such that the color signals on the color signal buses 27 to 29 are stored simultaneously in three stages of the column register 18 for each dot of the input image signal.

Fig. 11 shows a second embodiment of the invention. In the preceding first embodiment of Fig. 9, each row drive line $2_2\ell$ is provided for every two rows of display elements. In this second embodiment, however, each row drive line is provided for each display element row. That is, row drive lines $2_2\ell+1$, $2_2\ell+3$, ••• are provided additionally to the embodiment of Fig. 9. To each of these additional row drive lines are connected display elements on the opposite sides, i.e., on the upper and lower sides of the additional row drive line in the Figure. Each display element is also connected to the column drive lines or opposite sides thereof. In more specific, there are provided, on opposite sides of the row drive line, for example, $2_2\ell+1$, additional thin-film transistors (labeled by circles)- $4_2\ell+1,3n$, $4_2\ell+1,3n+2$, ••• , and $4_2\ell+1,3n+1$, $4_2\ell+1,3n+3$,••• on one sides of the respective display electrodes $1_2\ell,3n+1$, $1_2\ell,3n+3$, ••• , and $2_2\ell+2,3n$, $1_2\ell+2,3n+2$, ••• , opposite respectively from those thin-film transistors $4_2\ell,3n+1$, $4_2\ell,3n+3$, ••• and $4_2\ell+2,3n$, $4_2\ell+2,3n+2$, ••• shown in Fig. 9. These additional thin-film transistors on opposite sides of the additional row drive line $2_2\ell,+1$ have gates connected to the row drive line $2_2\ell,+1$, drains connected to the corresponding display electrodes and sources connected to the corresponding column drive lines on the sides of the respective display electrodes opposite from those column drive lines connected to the thin-film transistors having no circle label. That is, the thin-film transistors $4_2\ell+1,3n$, $4_2\ell+1,3n+2$, ••• , and $4_2\ell+1,3n+1$, ••• $4_2\ell+1,3n+3$, ••• have their drains connected to the respective opposite side display electrodes $1_2\ell,3n+1$, $1_2\ell,3n+3$, ••• and $1_2\ell+2,3n$, $1_2\ell+2,3n+2$, ••• , their sources connected to the respective column drive lines $3_{3n}$, $3_{3n+2}$, ••• , and $3_{3n+1}$, $3_{3n+3}$, ••• and their gates commonly connected to the row drive line $2_2\ell,+1$. In a similar manner, additional thin-film transistors are provided for each of the other additional row drive lines.

In either first or second embodiment, two rows, i.e., upper and lower side rows of display elements are connected to each row drive line, so that two rows of display elements can be displayed while a single row drive line is being selected. Thus, the row drive lines can be reduced in number to one hald compared to the row drive lines in the prior art arrangement shown in Fig. 2. This means that for the same period, during which each row drive line is selectively driven, the driving period for one frame can be reduced to one half, resulting in reduced flicker and improved quality of the displayed image. Alternatively, for the same frame display period, e.g., 1/60 second, the number of display element rows can be doubled to increase the resolution correspondingly. Further, for the same number of display element rows, the period of driving of one row drive line can be doubled compared to the prior art system. That is, the drive speed can be reduced to permit simpler construction of the peripheral circuits. Further, in the case of the liquid crystal display, the charging period for each of the display electrodes can be extended so that it is possible to obtain a display image having an improved contrast.

Although the number of column drive lines is doubled compared to the prior art system, the number of row drive lines is reduced to one half, so that the design and manufacture of the device will not become difficult.

Where the prior art planar display device is used for the color display of the type where each picture point is represented by a set of three color display, elements, the row drive line has to be driven twice for the display of one display row. In other words, the display device is scanned twice during one horizontal scanning cycle period of the image signal. Therefore, the correspondency to the image signal is unsatisfactory in view of displaying the image signal supplied for each horizontal scanning cycle period. According to the invention, the image signal supplied for each horizontal scanning cycle period is displayed by driving each row drive line only once for one horizontal scanning line period. Nevertheless, the display thus obtained for one display row consists of three-color display element sets as respective picture points. The display device according to the invention thus has satisfactory matching property with respect to the input of the image signal.

According to the invention, three color signals for each picture point can be simultaneously input to the column register 18 as mentioned earlier.

Further, it is possible to store three color signals for two or three picture points simultaneously in the column register 18.

For example, as shown in Fig. 12, it is possible that the color signal buses 27 to 29 are connected through a one-dot delay circuit 35 to color signal buses 36 to 38, and the color signals 27 to 29 and 36 to 38 are successsively and repeatedly connected to individual stages of the column register 18. In this case, the column register 18 is divided into groups each consisting of 6 stages, a horizontal sync pulse $H_{syn}$ is supplied to the first stage of a shift register 39 and shifted therethrough in response to the output of a frequency divider 41, which divides the frequency of a dot clock from a terminal 40 to one half, and writing of data in one of the groups of the column register 18 is effected according to the output of each stage of the shift register 39. In this way, the input image signal is stored six color signals for two picture dots at a time in the column register 18.

With the second embodiment shown in Fig. 11, it is possible to display one field, say, even field by three-color display-element sets for respective picture dots as shown by solid lines in Fig. 13 using the row drive lines $2_2\ell$, $2_2\ell+2$, ••• and then display one field, say, odd field by three-color display-element sets for respective picture dots as shown by phantom lines using the row drive lines $2_2\ell+1$, $2_2\ell+3$, ••• . By repeating the alternate displays shown by the solid and phantom lines in Fig. 13, it is possible to obtain a display well matched to the interlaced scanning image signal and also improve the resolution in the direction of the column drive lines.

Further, in the second embodiment twofold path is provided for the driving of each display element. That is, even if one of the two paths is defective, the display element may be driven through the other path. This means a corresponding increase in the production yield. While the above embodiments of the invention have concerned with the liquid crystal planar display devices, the invention is applicable to planar display devices based on light-emitting diodes or plasma display as well.

As for the driving of the liquid crystal, longer life can be ensured by AC driving. From this standpoint, it may be possible to adopt in the second embodiment (Fig. 11) to drive the liquid crystal with positive voltage for the column drive lines $3_{3n}$, $3_{3n+2}$, $3_{3n+4}$ •••and with negative voltage for the column drive lines $3_{3n+1}$, $3_{3n+3}$, $3_{3n+5}$, •••. However, when a certain column drive line $3_{3n}$ is disconnected, the portion of liquid crystal corresponding to display elements each connected to both the column drive lines $3_{3n}$and $3_{3n+1}$ on the side beyond the point of disconnection opposite from the power supply, is driven solely by the positive voltage through the column drive line $3_{3n}$. The life of this portion of liquid crystal would be thus shortened.

This drawback can be overcome by a driving scheme shown in Fig. 14. Let it be taken as an example of the display electrode $1_{2\ell},3n+1$ connected via thin-film transistors to the column drive lines $3_{3n}$ and $3_{3n+1}$ simultaneously driven by either positive or negative volatage. For the first field (odd field) the row drive line $2_{2\ell}+1$ is selected to turn ON the thin-film transistor $4_{2\ell}+1,3n$, whereby a negative voltage is applied across the liquid crystal at the display electrode $1_{2\ell},3n+1$ by negative voltage supplied from the line $3_{3n}$, for the second field (even field) the row drive line $2_{2\ell}$ is selected to turn ON the transistor $4_{2\ell},3n+1$, whereby a negative voltage is applied across the liquid crystal at the same display electrode by negative voltage supplied from the line $3_{3n+1}$, for the third field (odd field) the line $2_{2\ell}+1$ is selected to turn ON the transistor $4_{2\ell}+1,3n$, whereby a positive voltage is applied across the liquid crystal by positive voltage supplied from the line $3_{3n}$, and for the fourth field (even field) the line $2_{2\ell}$ is selected, whereby a negative voltage is applied across the liquid crystal by negative voltage supplied from the line $3_{3n+1}$. For the subsequent fields, the drive control is carried out as shown in Fig. 14. As will be seen from Fig. 14, the drive control sequence pattern repeats for every eight successive fields. The pattern shown in Fig. 14 is only an example of driving waveform, and it is also possible to use a pattern which is shifted in phase by one field period with respect to the pattern of Fig. 14. When applying a positive or negative voltage to the column drive lines, zero voltage is applied to the common electrode 4 (Fig. 1).

For the AC driving of the liquid crystal irrespective of the disconnection of a row drive line, the following procedure is effective. Taking the row drive lines $2_{2\ell}$ and $2_{2\ell}+1$ as an example, for the first field, during which the row drive line $2_{2\ell}+1$ is driven, a negative volatage is applied across the liquid crystal at the respective display electrodes supplied from all the selected column drive lines, for the second field, during which the row drive line $2_{2\ell}$ is driven, negative voltage is supplied to all the selected column drive lines, for the third field, during which the row drive line $2_{2\ell}+1$, is driven positive voltage is supplied to all the selected column drive lines, and for the fourth field negative voltage is supplied to all the selected column drive lines.

The waveform as shown in Fig. 14 may be obtained with an arrangement as shown in Fig. 15, for instance. The vertical sync pulse signal supplied from a terminal 51 is frequency divided into one half the frequency in a flip-flop 52. The $\overline{Q}$

and Q outputs of the flip-flop 52 are used to control gates 53 and 54 to separate the input vertical sync pulses into even and odd field pulses. The separated pulse signals are frequency divided into one half the frequency in respective flip-flops 55 and 56. The outputs of these flip-flops are ANDed in an AND gate 57. Meanwhile, the output of the flip-flop 56 is frequency divided into one half the frequency in a flip-flop 58. The outputs of the flip-flop 58 and AND gate 57 are exclusively ORed in an exclusive OR gate 59. As a result, an intended output is obtained at an output terminal 61.

## Claims

A planar display device comprising a plurality of display elements ($1_{2\ell}$,3n) arranged in rows and columns, a plurality of first row drive lines ($2_{2\ell}$) provided for and extending along respective rows of said display elements and a plurality of column drive lines ($3_{3n}$) provided for and extending along respective columns of said display elements, said first row drive lines and column drive lines being selectively driven to selectively activate said display elements,
CHARACTERIZED IN THAT
said first row drive lines each are provided for two adjacent rows of said display elements, said display elements on opposite sides of each said first row drive line ($2_{2\ell}$) being commonly connected to said first row drive line, said column drive lines being provided in pairs ($3_{3n}$, $3_{3n+1}$) each for each column of said display elements, every other ones of said display elements in said column being connected to one of said pair column drive lines, the other display elements in said column being connected to the other column drive line in the pair.

2.The planar display device according to claim 1, which further comprises second row drive lines each provided for and extending between two adjacent display element rows between adjacent said first row drive lines, corresponding ones of said display elements on opposite sides of each said second row drive line being commonly connected to said each second row drive line, each of said display elements in each column being connected to both said column drive lines in the pair for the corresponding column of said display elements.

3. The planar display device according to claim 1, which further comprises row drive means for driving said plurality of first row drive lines one after another in synchronism with the horizontal scanning cycle of an image signal to be displayed and column drive means supplied with said image signal for one scanning lines and having stages equal in number to said plurality of column drive lines for driving said column drive lines according to the outputs of corresponding said stages.

4. The planar display device according to claim 2 or 3, wherein red, green and blue color filters are provided on respective said display elements to form three-color display element sets such that said color filters are substantially uniformly distributed as a whole, two of the three color display elements in each set in a column and the other color display element in an adjacent column constituting one of picture points with respect to a first row drive line.

5. The planar display device according to claim 4, wherein said input image signal consists of serial pixel signals each consisting of parallel, red, green and blue color signals, and said device further comprises a shift register supplied with the horizontal sync signal for shifting signals under control of a clock signal at three times the frequency of the pixel signals, first to third color signal buses, through which the three color signals are successively and repeatedly supplied to corresponding stages of said column drive means according to data shifted through said shift register, and means for switching the connection of input lines, to which said red, green and blue signals are supplied, and said first to third color signal buses, for each said horizontal sync signal.

6. The planar display device according to one of claims 2 and 4, which further comprises means for driving said first row drive lines for even fields of said image signal and driving said second row drive lines for odd fields of said image signal.

7. The planar display device according to claim4, which further comprises first to third color signal buses, to which red, green and blue color signals are supplied, fourth to sixth color signal buses, to which said red, green and blue color signals are supplied after being delayed for one pixel clock period, a shift register, to which horizontal sync pulses of said image signal are supplied as data and a clock signal at one half the frequency of the pixel clock of said image signal is supplied as a shift clock, and a plurality of column registers each supplied with color signals on said first to sixth color signal buses in response to the stage outputs of said shift register for supplying six outputs of each said column register to corresponding ones of said column drive lines.

8. The planar display device according to one of claims 1 to 5, wherein said planar display device is a liquid crystal display device, and said display elements are constituted by display electrodes arranged in row and columns in said liquid crystal display device, thin-film transistors having respective drains connected to said display electrodes. respective gates connected to said first and second

row drive lines and respective sources connected to said column drive lines, and a common electrode facing said display electrodes via a liquid crystal.

9. The planar display device according to one of claims 1 to 5, wherein said column drive lines in each pair are provided on the opposite sides of each column of display elements.

10. The planar display device according to claim 1, which further comprises liquid crystal AC drive means for driving the liquid crystal in first and second different frames for every eight successive fields, a voltage of one polarity being applied across said liquid crystal for the odd and even fields in said first kind of frame, voltages of opposite polarities being applied across said liquid crystal for the respective odd and even fields in said second kind of frame, said first and second frames occurring alternately, the polarity of the voltage applied across said liquid crystal being inverted when said first and second kinds of frames are changed.

11. The planar display device according to claim 10, wherein said liquid crystal AC drive means includes means for separating vertical sync pulses into those for even fields and those for odd fields, first and second frequency divider means for frequency dividing said separated pulses into one half the frequency, an AND gate for ANDing the outputs of said frequency divider means, third frequency divider means for frequency dividing the output of said second frequency divider means into one half, and an exclusive OR gate for exclusively ORing the outputs of said third frequency divider means and said AND gate.

FIG. 1
PRIOR ART

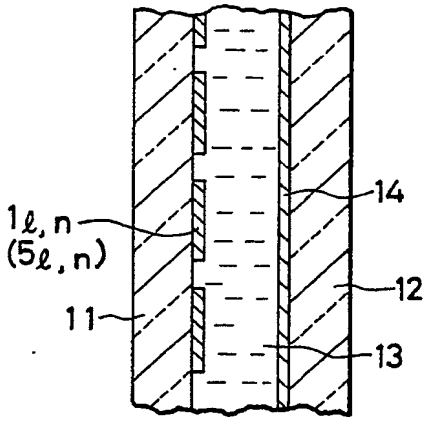



FIG. 2
PRIOR ART

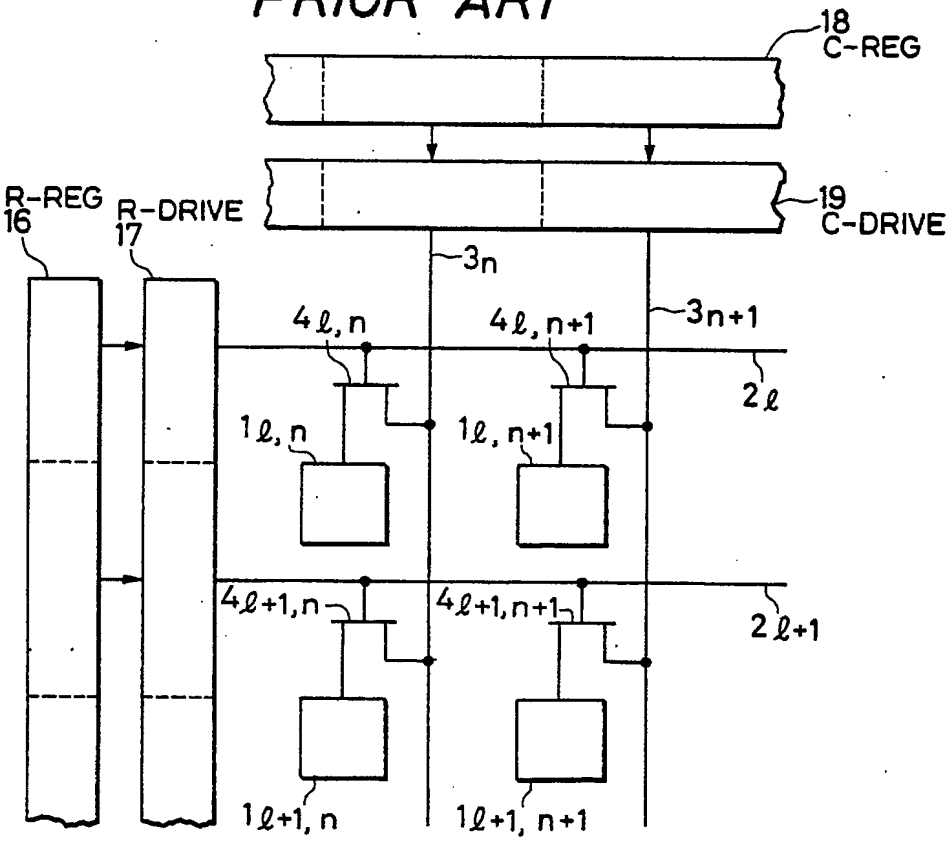


FIG. 3
PRIOR ART

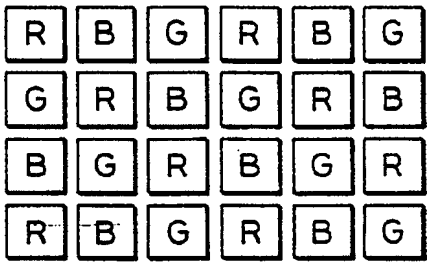



FIG. 4
PRIOR ART



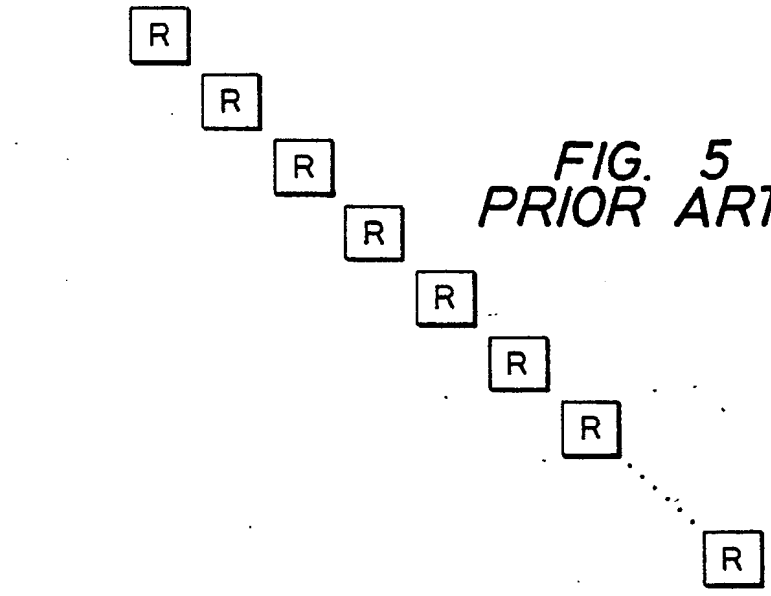




FIG. 5
PRIOR ART

FIG. 6
PROR ART

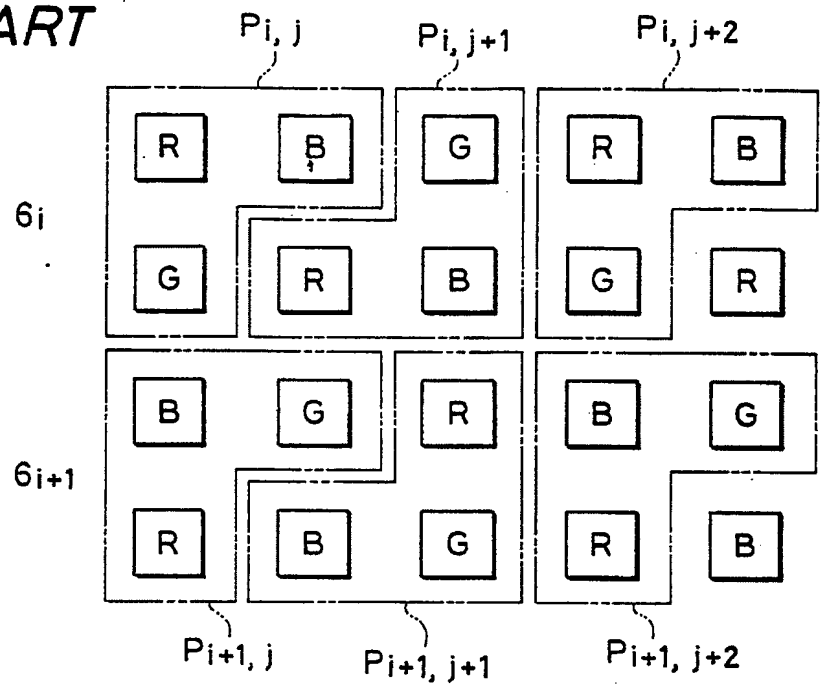



FIG. 7
PRIOR ART

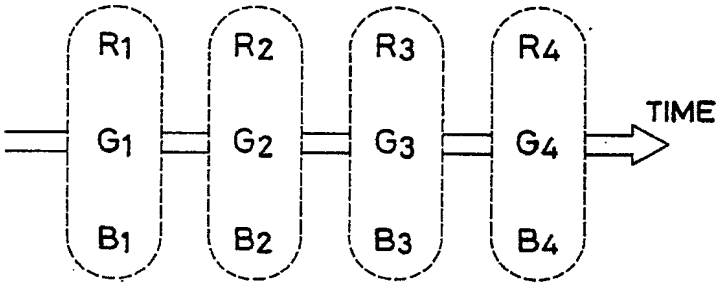



FIG. 8A
PRIOR ART

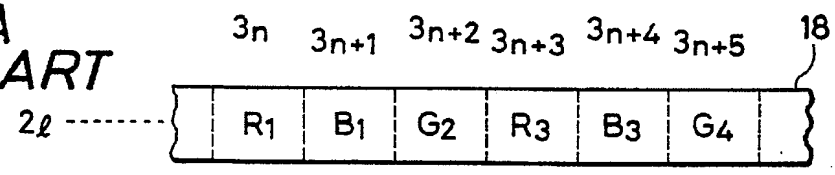



FIG. 8B
PRIOR ART

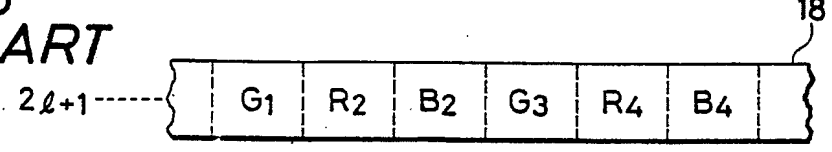
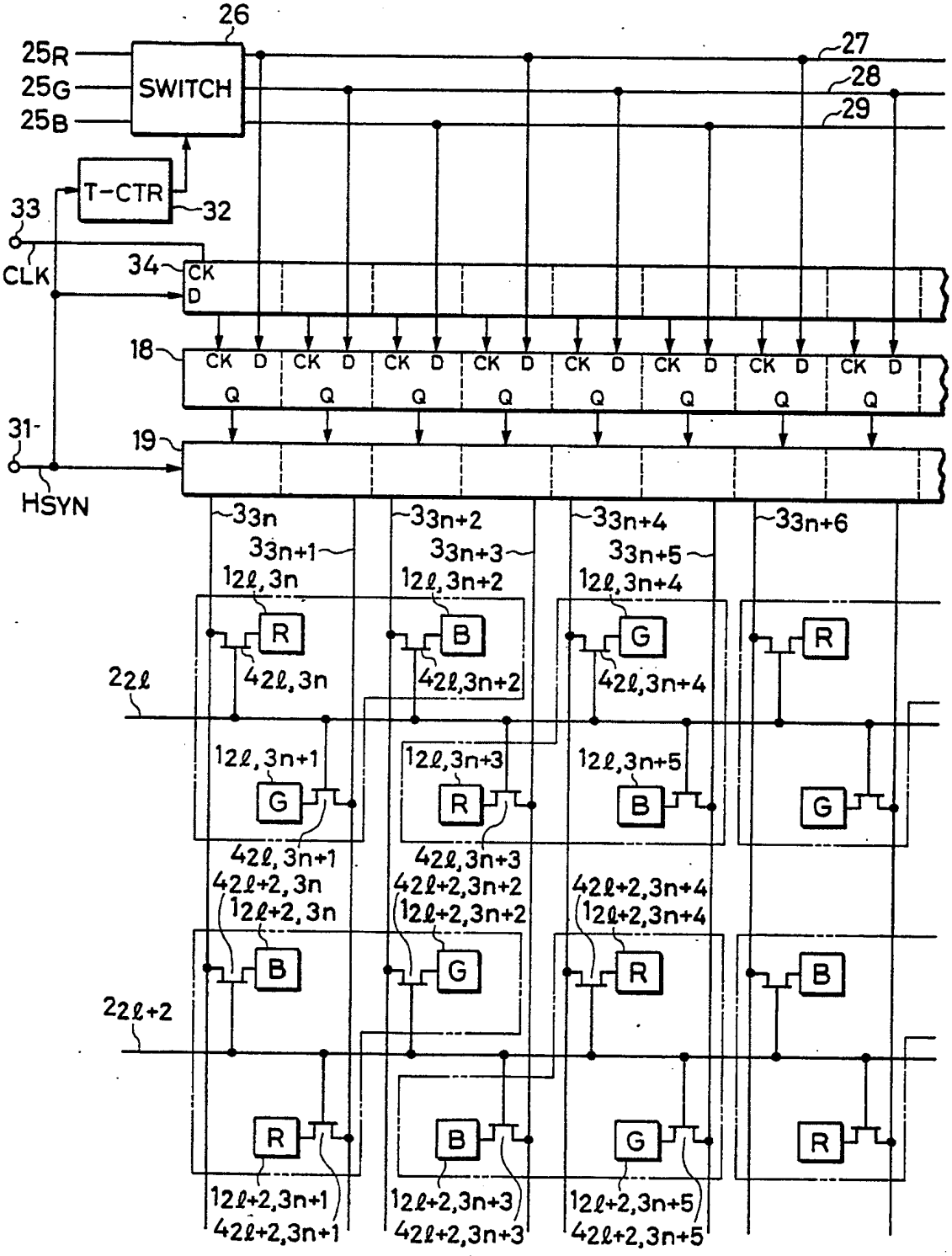


FIG. 9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25G
25B
SWITCH
27
28
29
T-CTR
32
33
CLK
34
CK
D
18
CK D
Q
31
19
HSYN
33n
33n+1
33n+2
33n+3
33n+4
33n+5
33n+6
12ℓ,3n
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12ℓ,3n+1
12ℓ,3n+3
12ℓ,3n+5
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R
G
B

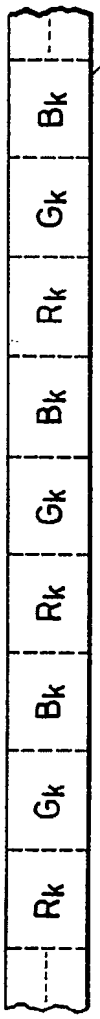



FIG. 10A


FIG. 10B


FIG. 10C

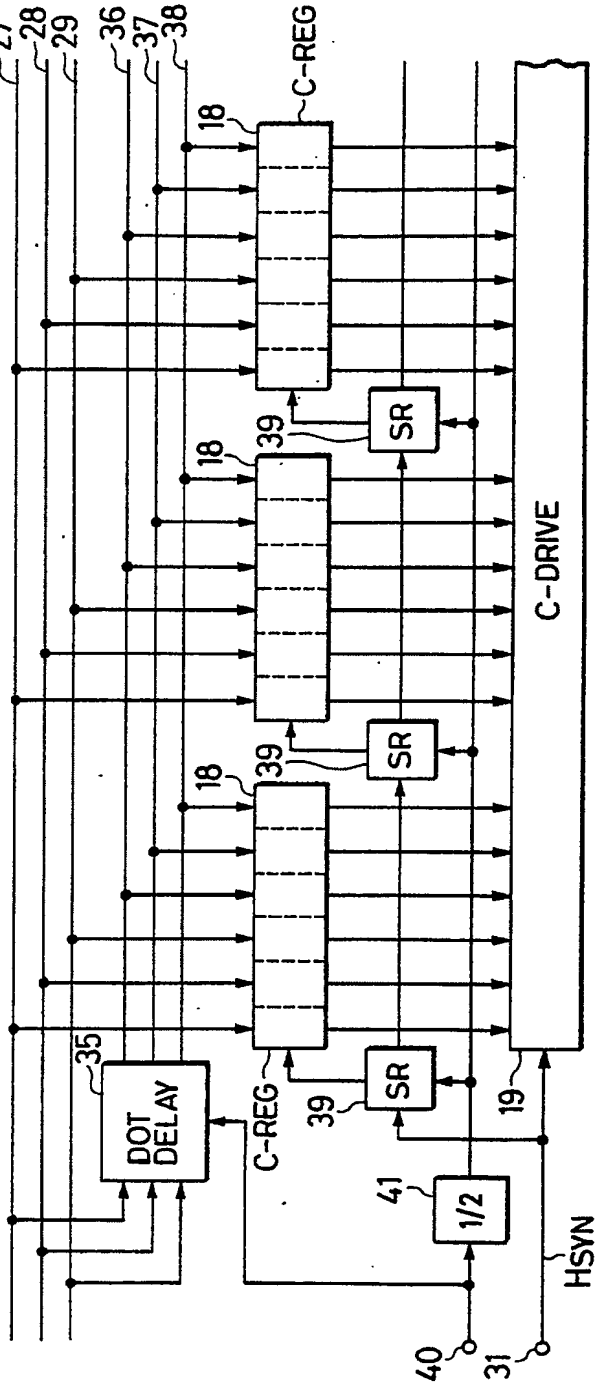
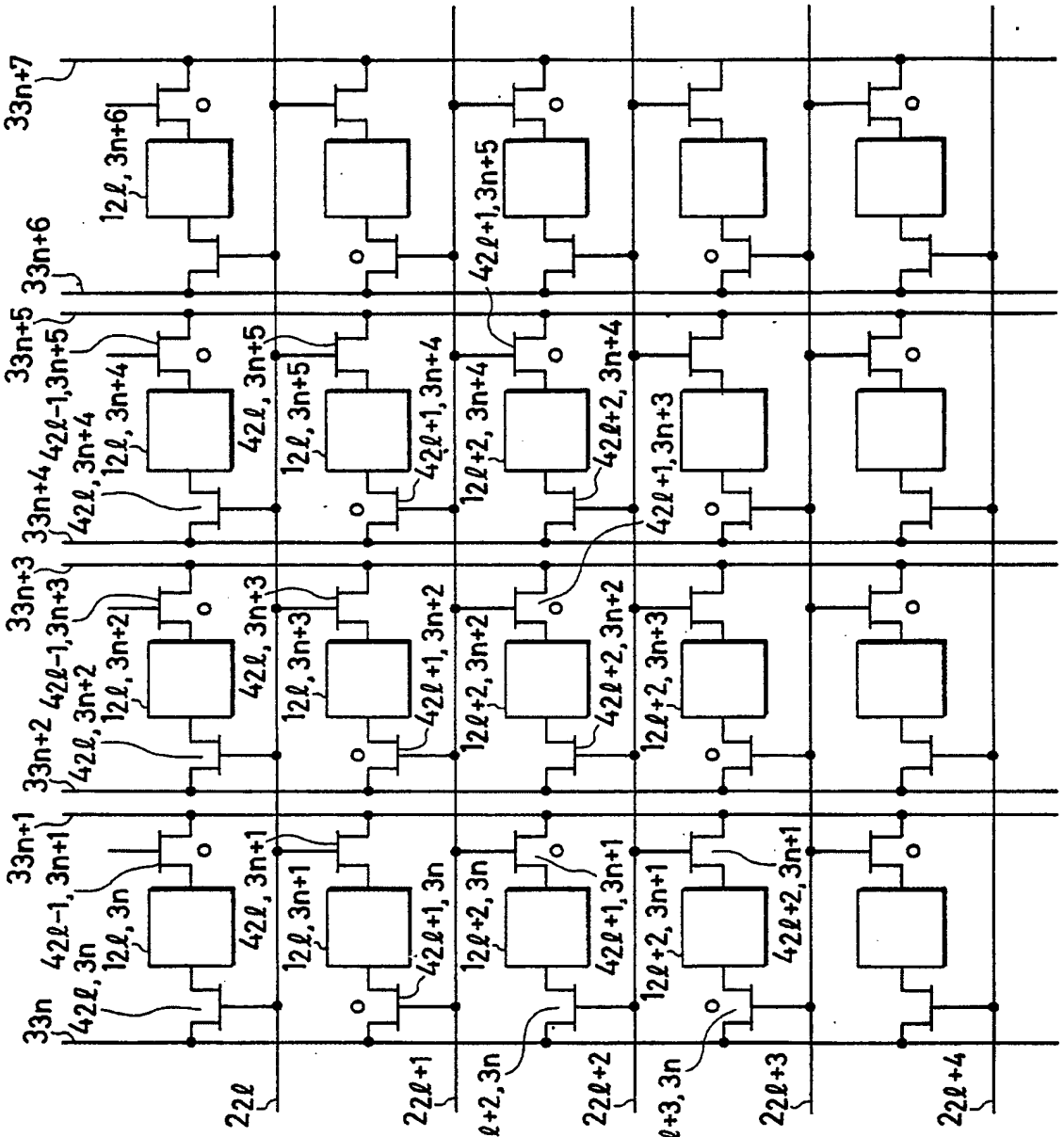



FIG. 12

FIG. 11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12ℓ, 3n+6
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22ℓ+1
22ℓ+2
22ℓ+3
22ℓ+4

FIG. 13

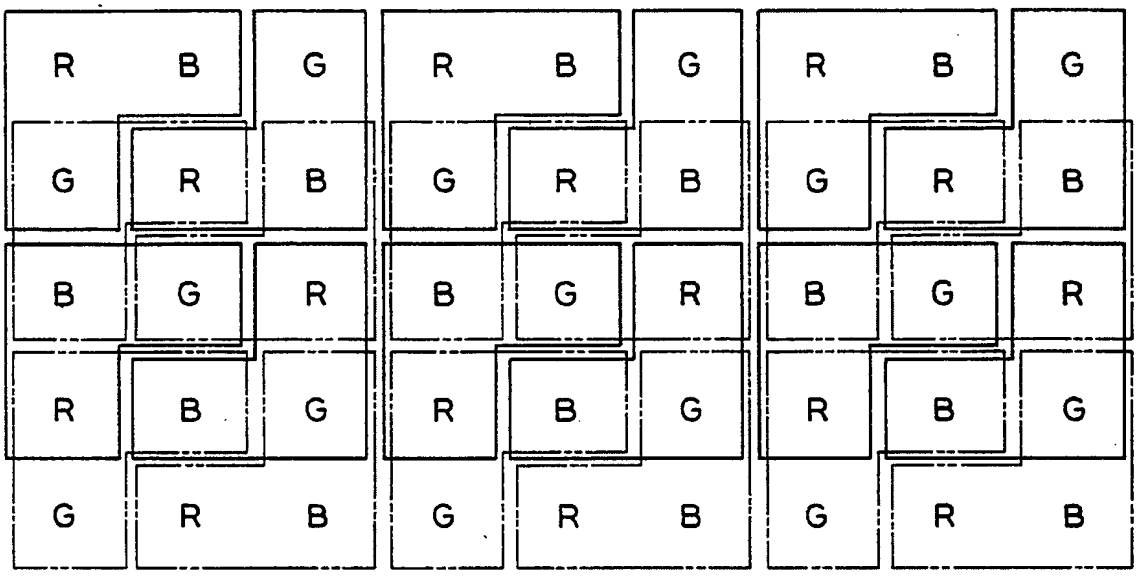



FIG. 14

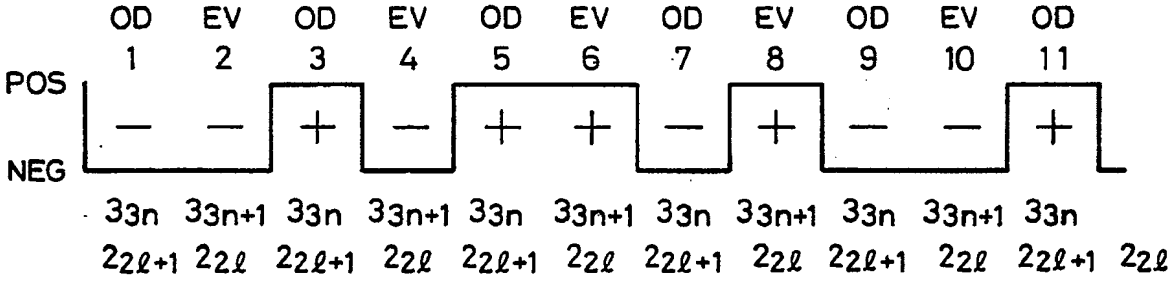
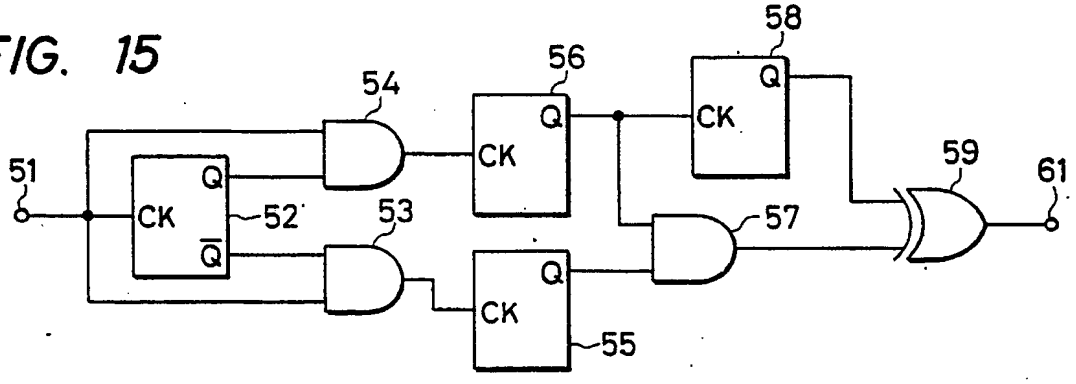



FIG. 15



European Patent Office

# EUROPEAN SEARCH REPORT

Application number

EP 87 10 0148

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.4) |
|---|---|---|---|
| A | EP-A-0 167 408 (SHARP KABUSHIKI KAISHA) * Figure 6; abstract; page 20, line 15 - page 21, line 12 * | 1 | G 09 G 3/36<br>G 09 G 3/20 |
| A | EP-A-0 181 598 (CANON KABUSHIKI KAISHA) * Figure 1; abstract; page 8, lines 21-27 * | 1 | |

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

G 09 G

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 28-09-1987 | VAN ROOST L.L.A. |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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